

ABSTRACT

Trench and stacked capacitors are commonly used in the construction of DRAMs utilized in electronic devices. Conventional methods of manufacture typically result in capacitor structures having relatively smooth sidewall profiles which are integrated into a capacitor structure. The present invention provides a novel method by which the capacitance density of both trench and stacked capacitors can be increased, without increasing the footprint or depth of the capacitor structure, by increasing the surface area of the sidewall profiles of the capacitor structures using an iterative etch process that comprises an isotropic plasma etching step to achieve an enlarged sidewall profile.

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